The Design of High-Throughput Asynchronous Pipelines

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ABSTRACT

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Clocked or *synchronous* design has traditionally been used for nearly all digital systems. However, it is now facing significant challenges as clock rates reach several GigaHertz, chip sizes increase, and the demand for low power and modular design become paramount. An alternative paradigm is clockless or *asynchronous* design, which has several potential advantages towards meeting these challenges.

This thesis focuses on the design of very high-speed asynchronous systems. A more specific focus of this thesis is on high-throughput asynchronous pipelines, since pipelining is at the heart of most high-performance systems.

This thesis contributes four new asynchronous pipeline styles: "lookahead," "high-capacity," "MOUSETRAP" and "dynamic GasP" pipelines. The styles differ from each other in many aspects, such as protocols, storage capacity, implementation style, and timing assumptions. The new styles are capable of multi-GigaHertz throughputs in today's silicon technology (*e.g.,* 0.13-0.18 micron), yet each style has a simple implementation. High throughputs are obtained through efficient pipelining of systems at a fine granularity, though the pipeline styles are also useful for coarser-grain applications.

The basic pipeline styles are extended to address several issues that arise in practice while designing real-world systems. In particular, the styles are generalized to handle a greater variety of architectures (*e.g.,* datapaths with forks and joins), and to robustly interface with arbitrary-speed environments.

Finally, the approaches of this thesis are validated by designing and fabricating real VLSI subsystems, including: simple FIFO's, pipelined adders, and an experimental digital FIR filter chip. All chips were tested to be fully functional; throughputs of over 2.4 GHz for the FIFO's, and up to 1.3 GHz for the FIR filter, were obtained in an IBM 0.18 micron technology.